



Shaoxing Yuli Semiconductor CO., LTD

绍兴宇力半导体有限公司



## U3406 Data Sheet

V 0.5

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## ■ General Description

The U3406 400V synchronous buck controller regulates from a high input voltage source or from an input rail subject to high voltage transients, minimizing the need for external surge suppression components. A high-side switch minimum on-time of 60 ns gives large step-down ratios, enabling the direct step-down conversion from a 100V nominal input to low-voltage rails for reduced system complexity and solution cost. The U3406 continues to operate during input voltage dips as low as 8.5V, at nearly 100% duty cycle if needed, making it an excellent choice for high-performance 100V battery automotive applications, ADAS (surround view ECU) and HEV/EV systems.

Forced-PWM (FPWM) operation eliminates switching frequency variation to minimize EMI, while user-selectable diode emulation lowers current consumption at light-load conditions. Measuring the voltage drop across the low-side MOSFET or with an optional current sense resistor gives cycle-by-cycle overcurrent protection.

## ■ Applications

- High-Power Automotive DC/DC Regulator
- Automotive Motor Drives, ADAS
- HEV/EV Power Compliant to LV-148

## ■ Key Features

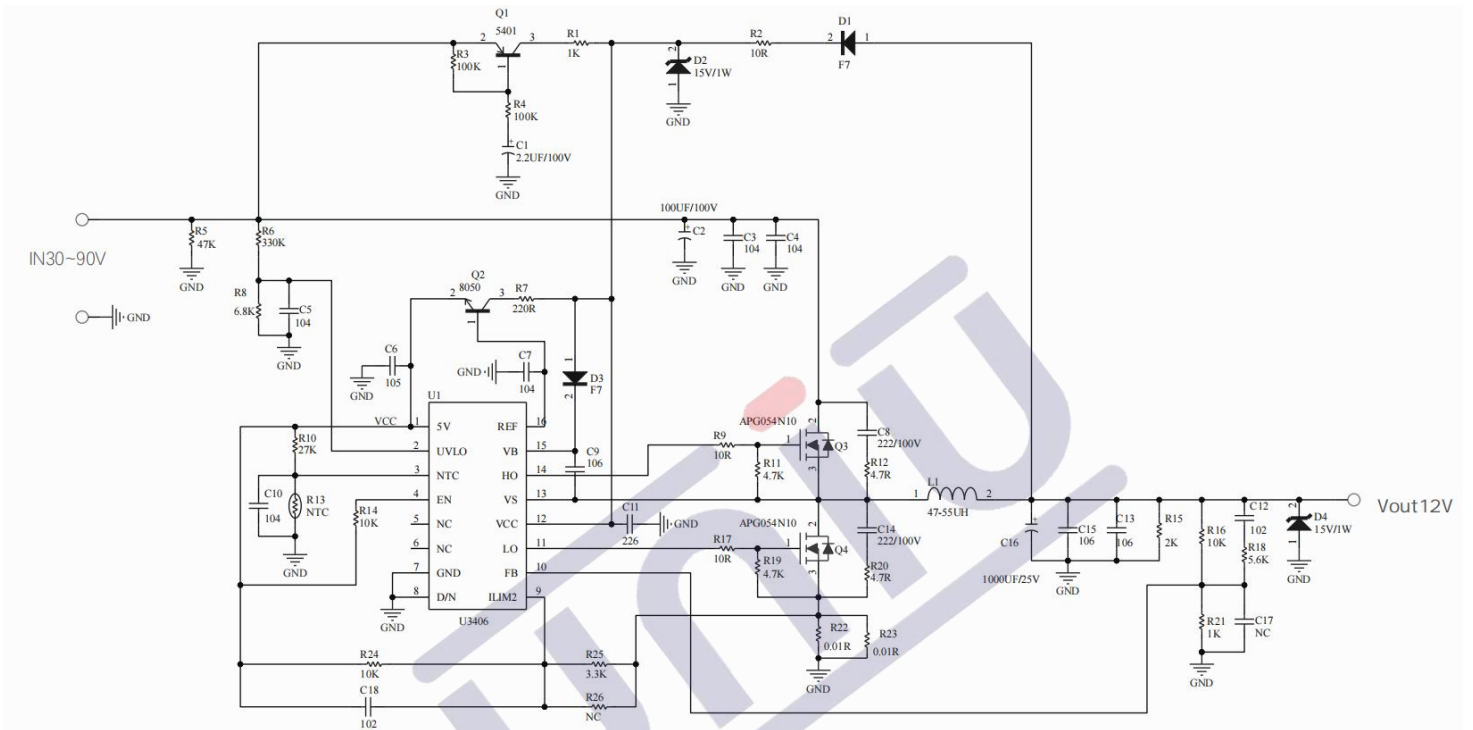
- Device Temperature Grade 1: -40°C to +125°C Ambient Temperature Range
- Versatile Synchronous Buck DC/DC Controller
  - Wide Input Voltage Range of 9.5V to 400V
  - Adjustable Output Voltage From 1.25V to 280V
  - Voltage-mode Control With Line Feedforward
- Three-stage frequency conversion
- 60ns Minimum On-Time for High  $V_{IN} / V_{OUT}$  Ratio
- 180ns Minimum Off-Time for Low Dropout
- 1.1V Reference With  $\pm 1\%$  Feedback Accuracy
- 8.5V Gate Drivers for Standard  $V_{TH}$  MOSFETs
  - 220ns Adaptive Dead-Time Control
  - 2A Source and 2.5A Sink Capability
- Inherent Protection Features for Robust Design
  - Hiccup-Mode Overcurrent Protection
  - Input UVLO With Hysteresis
  - VCC and Gate-Drive UVLO Protection
  - Thermal Shutdown Protection With Hysteresis
- 16-Pin SOP Package With Wettable Flanks
- Create a Custom Design Using the U3406 With UNI-SEMI<sup>®</sup> Power Designer

■ Device Information<sup>(1)</sup>

Part Number	Package	Body Size (Nom)
U3406	SOP(16)	10mm × 6.3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet

■ Simple application diagram



■ Output Power Table

Part Number	Package	VIN	IO+/IO-	OUT
U3406	SOP-16	9.5~400V	2A/2.5A	ADJ

Note:

- 1.Default for Buck Converter Application
- 2.The practical output power is determined by the output voltage and thermal condition

## ■ Description (continued)

The U3406 voltage-mode controller with line feedforward drives external high-side and low-side N-channel power switches with robust 8.5V gate drivers suitable for standard-threshold MOSFETs. Adaptively-timed gate drivers with 2A source and 2.5A sink capability minimize body diode conduction during switching transitions, reducing switching losses and improving thermal performance when driving MOSFETs at high input voltage and high frequency. The U3406 can be powered from the output of the switching regulator or another available source, further improving efficiency.

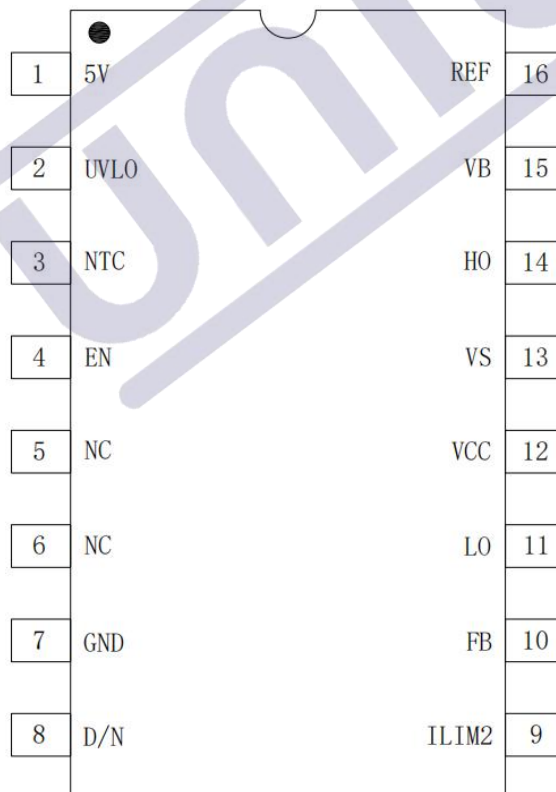
Additional features of the U3406 include a configurable soft start, an open-drain power-good monitor for fault reporting and output- monitoring, monotonic start-up into prebiased loads, integrated VCC bias supply regulator and bootstrap diode, external power supply tracking, precision enable input with hysteresis for adjustable line undervoltage lockout (UVLO), hiccup-mode overload protection, and thermal shutdown protection with automatic recovery.

The U3406 controller is offered in a 10mm × 6.3mm thermally enhanced, 16-pin SOP package with additional spacing for high-voltage pins and wettable flanks for optical inspection of solder joint fillets.

## ■ Pin Configuration and Functions

RGY Package 16-Pin SOP With Wettable Flanks

Top View



## ■ Pin Functions

Pin		I/O <sup>(1)</sup>	Description
NO.	Name		
1	5V	O	The Pin is VCC 5V
2	UVLO	I	Input voltage detection.
3	NTC	P	Enable input and under voltage lockout programming pin. If the EN/UVLO voltage is below 1V, Power on again after temperature protection
4	EN	I	Test PIN& Standby IO port
5	NC	I	NC
6	NC	I	NC
7	GND	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low- side MOSFET or the ground side of a shunt resistor.
8	D/N	I	Delay setting , built-in 26K pull-up resistance, can adjust the delay time with external pull-down resistance, 0.1V is 1 second, the maximum support 24 seconds.
9	ILIM2	I	Current detection in three-wire connection. Ultra-low overload protection below 1V, short circuit protection below 0.7V
10	FB	I	Feedback input. The regulation threshold at the FB pin is nominally 1.1V.
11	LO	P	Low-side MOSFET gate drive output.
12	VCC	O	Power input
13	VS	P	Switching node of the buck controller.
14	HO	P	High-side MOSFET gate drive output.
15	VB	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap (boot) capacitor.
16	REF	O	the reference for VCC5V.

(1) P = Power, G = Ground, I = Input, O = Output.

## ● Electrical Characteristics

Typical values correspond to  $T_J = 25^\circ\text{C}$ . Minimum and maximum limits apply over the  $-20^\circ\text{C}$  to  $80^\circ\text{C}$  junction temperature range unless otherwise stated.  $V_{IN}=48\text{V}$ ,  $V_{CC}=12\text{V}$ ,  $V_{EN}/UVLO=5\text{V}$ , unless otherwise stated<sup>(1)(2)</sup>

Item	Parameter	Test Conditions	Min	Typ	Max	Unit
Input Supply						
$V_{CC}$	Operating input voltage range	$I_{VCC} \leq 10\text{mA}$ at $V_{VIN} = 12\text{V}$	10	—	25	V
$I_{Q-RUN}$	Operating input current, not switching	$V_{EN}/UVLO = 5\text{V}$ ,	—	1.8	2.1	mA
$I_{Q-STBY}$	Standby input current	$V_{EN}/UVLO = 5\text{V}$	—	1.75	2	mA
$I_{Q-SDN}$	Shutdown input current	$V_{EN}/UVLO = 0\text{V}$ , $V_{VCC} < 1\text{V}$	—	13.5	30	$\mu\text{A}$
REF/VCC Regulator						
$V_{REF}$	REF regulation voltage	$V_{CT1} = 0\text{V}$ , $24\text{V} \leq V_{VIN} \leq 100\text{V}$ , $0\text{mA} < I_{VCC} \leq 20\text{mA}$	—	5	—	V
$I_{SC-LDO}$	REF short-circuit current	$V_{REF} = 0\text{V}$ $V_{CC}=12\text{V}$	—	50	—	mA
$V_{VCC-UV}$	VCC undervoltage threshold	$V_{VCC}$ rising	—	8.5	—	V
Enable And Input UVLO						
$V_{EN}$	Standby to operating threshold	$V_{EN}/UVLO}$ rising	—	1	—	V
$I_{EN-HYS}$	Standby to operating hysteresis	$V_{EN}/UVLO = 1.5\text{V}$	9	10	11	$\mu\text{A}$
FB Reference						
$V_{REF}$	FB reference voltage		—	1100	—	mV
AVOL	DC gain		—	94	—	dB
GBW	Unity gain bandwidth		—	5	—	MHz
Current renferance						
$V_{lim2}$	I limit2 Reference Voltage	$V_{CC}=12\text{V}$	—	1	—	V
Oscillator						
$F_{SW1}$	Oscillator Frequency – 1	$V_{IN}=50\text{V}$	—	55	—	kHz
PWM Control						
$t_{ON(MIN)}$	Minimum controllable on-time	$V_{BST} - V_{SW} = 7\text{V}$ , HO 50% to 50%	—	160	—	ns
$t_{OFF(MIN)}$	Minimum off-time	$V_{BST} - V_{SW} = 7\text{V}$ , HO 50% to 50%	—	132	—	ns
DC <sub>55kHz</sub>	Maximum duty cycle	$F_{SW} = 55\text{kHz}$ , $6\text{V} \leq V_{VIN} \leq 60\text{V}$	—	70%	—	—
Gate Drivers						
$I_{HOH}$ , $I_{LOH}$	HO, LO source current	$V_{BST} - V_{SW} = 7\text{V}$ , HO=SW, LO=AGND	—	2.0	—	A
$I_{HOL}$ , $I_{LOL}$	HO, LO sink current	$V_{BST} - V_{SW} = 7\text{V}$ , HO=BST, LO=VCC	—	2.5	—	A
Thermal Shutdown						
$T_{SD}$	Thermal shutdown threshold	$T_J$ rising	—	175	—	$^\circ\text{C}$
$T_{SD-HYS}$	Thermal shutdown hysteresis		—	20	—	$^\circ\text{C}$

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

(2) The junction temperature ( $T_J$  in  $^\circ\text{C}$ ) is calculated from the ambient temperature ( $T_A$  in  $^\circ\text{C}$ ) and power dissipation ( $P_D$  in Watts) as follows:

$$T_J = T_A + (P_D \cdot R_{\theta JA}) \text{ where } R_{\theta JA} \text{ (in } ^\circ\text{C/W) is the package thermal impedance provided in Thermal Information.}$$

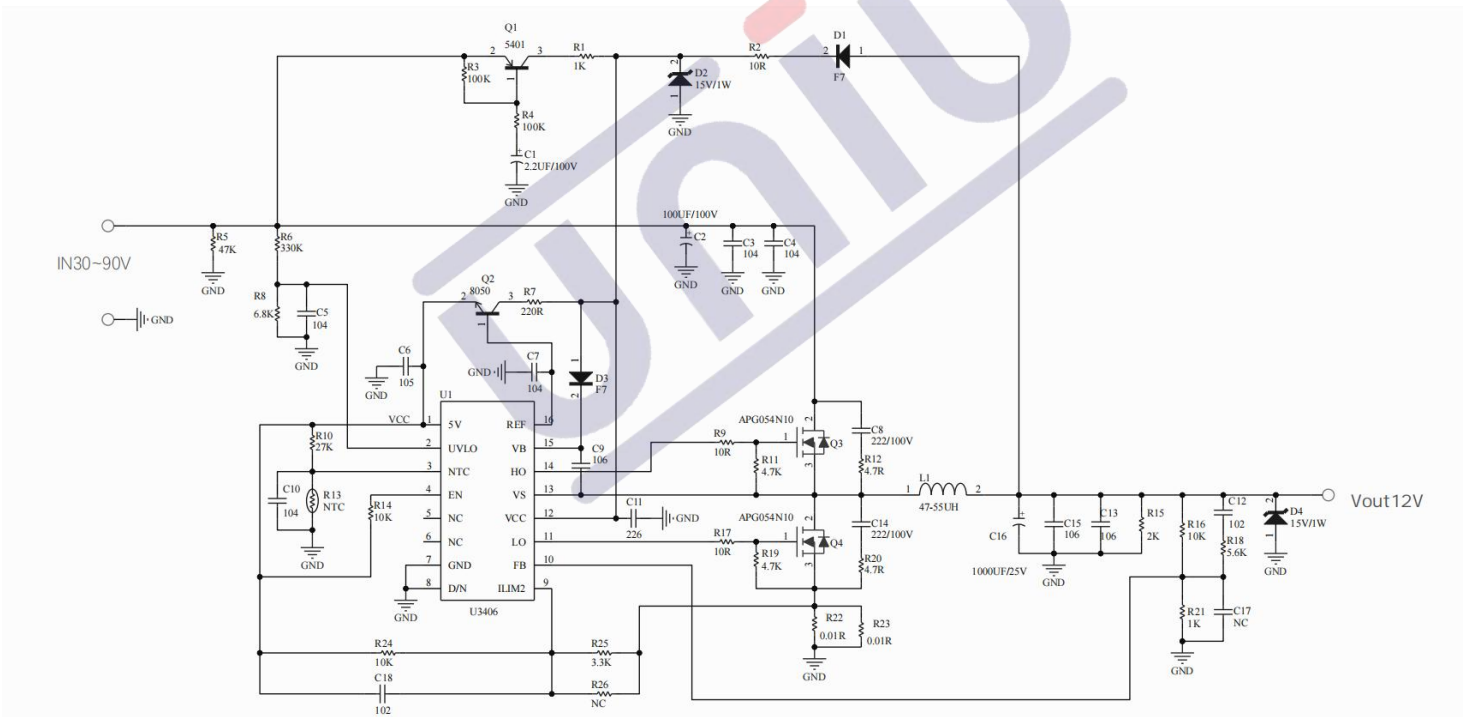
● Switching Characteristics

Typical values correspond to  $T_J = 25^{\circ}\text{C}$

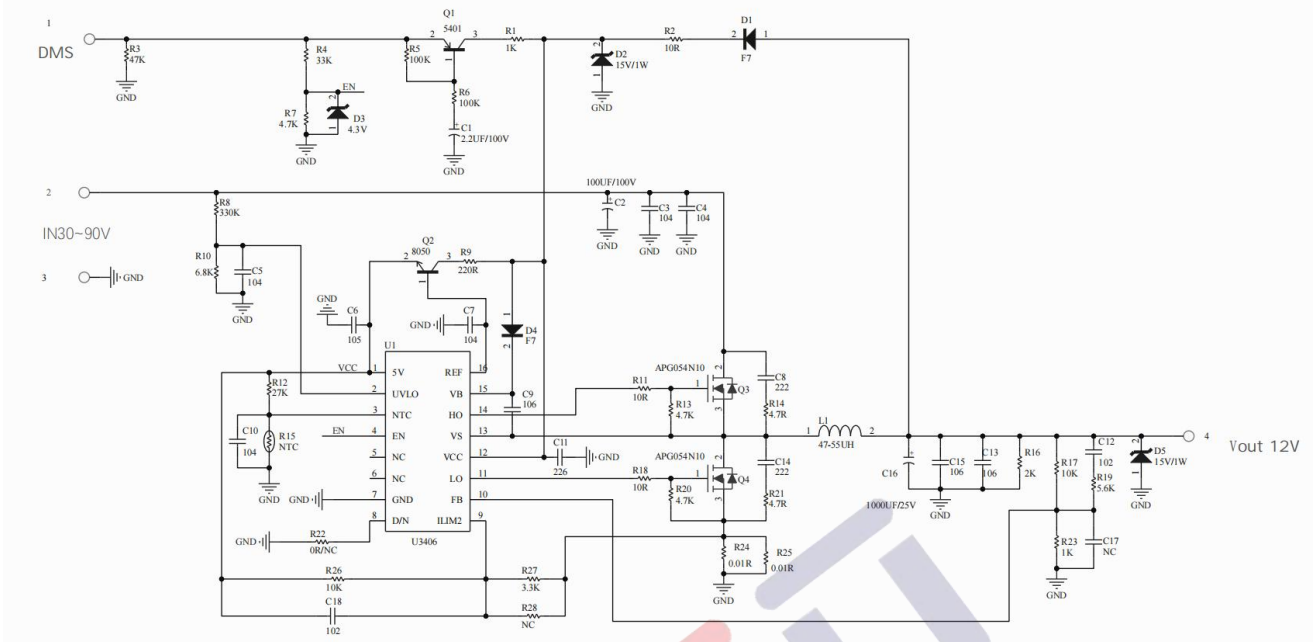
Item	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{HO-TR}$ $T_{LO-TR}$	HO, LO rise times	$V_{BST} - V_{SW} = 7\text{ V}$ , $C_{LOAD} = 1\text{ nF}$ , 20% to 80%	—	25	35	ns
$T_{HO-TF}$ $T_{LO-TF}$	HO, LO fall times	$V_{BST} - V_{SW} = 7\text{ V}$ , $C_{LOAD} = 1\text{ nF}$ , 80% to 20%	—	—	25	ns
$T_{HO-DT}$	HO turn-on dead time	$V_{BST} - V_{SW} = 7\text{ V}$ , LO off to HO on, 50% to 50%	—	300	—	ns
$T_{LO-DT}$	LO turn-on dead time	$V_{BST} - V_{SW} = 7\text{ V}$ , HO off to LO on, 50% to 50%	—	300	—	ns

■ Typical Application

APP1: Three-wire circuit diagram(no electric door lock)



APP2:Four-wire circuit diagram (electric door lock)

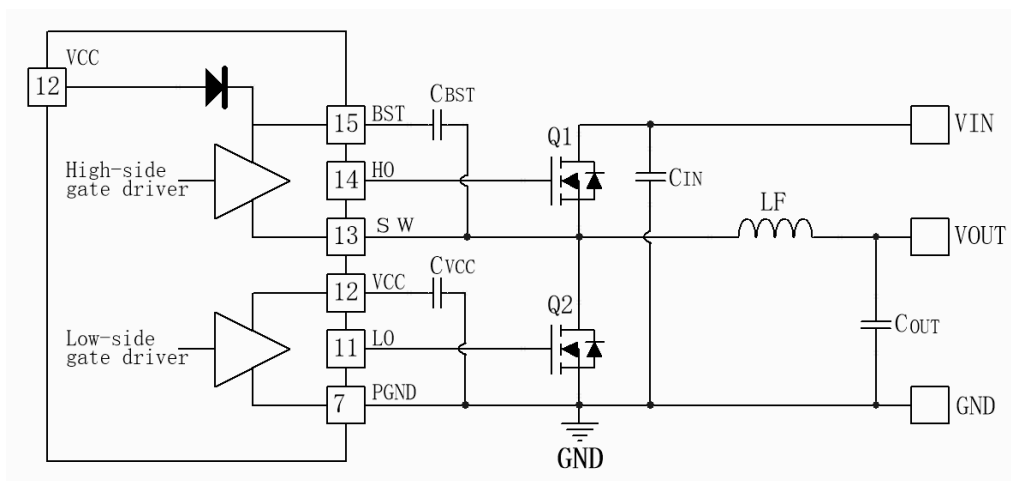


■ Layout

● Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the U3406. The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of Figure 70. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop 1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by 2 and 3.

DC/DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops



## 1、Version Record

Date	Rev.	Description
2022/09/28	0.1	First Release
2023/10/08	0.2	Update the application schematic diagram
2023/11/12	0.3	Optimization parameters and application schematic diagram
2023/12/30	0.4	Optimize parameters and functions
2024/05/15	0.5	Optimize parameters and functions

## 2、Contact

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